REMARKS

Claims 1-13, 19 and 20 are pending in this application, of which claims 4-13, 19 and 20 have been withdrawn from consideration. Claim 2 has been canceled. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Claim 1 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action.

Objections to the Title

The title of the invention has been objected to because it allegedly is not descriptive.

Accordingly, the title has been amended to read: "WAFER-LEVEL PACKAGE WITH TEST TERMINALS".

Rejections under 35 USC §102(b)

Claims 1-3 are rejected under 35 USC §102(b) as being anticipated by Frei et al (U.S. Patent No. 5,342,999).

Claim 1 has been amended to recite "at least one redistribution trace provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip

terminals and a second end of said redistribution trace being extended out of said semiconductor chip circuit forming region to a position offset from said one of said test chip terminals; at least one testing member provided in an outer region of said semiconductor chip circuit forming region of said semiconductor wafer, said second end of said redistribution trace being connected to said at least one testing member; an insulating material covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material, and a sealing resin provided on said insulating material such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin."

The Examiner alleged that Figs. 10 and 13 of Frei show a wafer-level package. Figs. 10 and 13 of Frei, however, show a multi-chip module board but do not show the wafer-level package of the present invention.

The Examiner also alleged that one of elements 26 of Frei corresponds to at least one non-test chip terminal. Elements 26 of Frei, however, are holes 26 punched through sheets (column 5, lines 41-44). According to the present invention, the distribution trace connected to a test terminal is extended out of the semiconductor chip circuit forming region. In other words, a first end of the redistribution trace is connected to one of the test chip terminals and a second end of the redistribution trace is extended out to a position offset from the test chip terminal.

The Examiner did not specify which element corresponds to the test chip terminal. The Examiner also failed to point out which portion teaches the recitation that the distribution trace connected to a test terminal is extended out of the semiconductor chip circuit forming region.

The Examiner also asserted that Frei et al discloses "at least one redistribution trace **(one of 70s)** provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals; at least one testing member **(one of 72s)** provided in an outer region of said semiconductor chip circuit forming region, said second end of said redistribution trace being connected to said least one testing member; and an insulating material **58** covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material."

Although Fig. 13 of Frei et al may appear to be similar to Fig. 1 of the present application, the difference becomes clear when the cross sectional view of Fig. 16 of Frei et al is compared with Fig. 2 of the present application. Frei et al describes as follows:

> FIG. 15 shows a cross sectional side view of a single carrier 10 from array 20 (see FIG. 2). At the stage depicted in FIG. 15, **coating 58 has been etched to form pads 68 of pad constellation 66b, traces 70, and land areas 72** (see FIG. 13). For clarity, FIG. 15 omits metallization from the interior of vias 56. . . . .
>
> FIG. 16 shows a cross sectional side view of a single carrier 10 and die 60 after an attachment stage. Preferably, conductive bumps 74 are welded to pads 68 by the use of a conventional thermal compression

> process which slightly raises temperatures while applying compression pressures preferably around 100 psi. This couples the N bond pads 62 of die 60 to the N pads 68 of carrier 10. In the preferred embodiment, die 60 is compressed with carrier 10 so that around a one mil gap remains between die 60 and carrier 10. The use of gold as **conductive coating 58** on surface 42 of carrier 10 and the use of the above-discussed alloy for conductive bumps 74 results in a relatively high temperature joint, wherein melting should not occur below 300 °C. Preferably, any number of dice 60 are attached to carriers 10 within array 20 (see FIG. 2) during this stage.

(Column 11, lines 35-61).

Thus, in Frei et al, trace 70, referred to by the Examiner as the **"redistribution trace" is NOT provided on the semiconductor wafer**. Also, land area 72, referred to by the Examiner as the **"testing member" is NOT provided in an outer region of said semiconductor chip circuit forming region of said wafer**. Moreover, coating 58, referred to by the Examiner as the "**insulating material** covering at least said redistribution trace" is **NOT insulating but conductive**.

Therefore, Frei et al does not teach or suggest "at least one redistribution trace provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals; at least one testing member provided in an outer region of said semiconductor chip circuit forming region, said second end of said redistribution trace being connected to said least one testing member; and an insulating material covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material."

Moreover, Claim 1 has been amended to further recite "a sealing resin provided on said insulating material such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin." Frei et al does not teach or suggest these recitations, either.

For at least these reasons, claim 1 patentably distinguishes over Frei et al. Claims 2 and 3, directly depending from claim 1, also patentably distinguish over the cited reference for at least the same reasons.

Claims 1-3 are rejected under 35 USC §102(b) as being anticipated by Wojnarowski(U.S. Patent No. 5,366,906).

As already mentioned, claim 1 has been amended to recite "a **sealing resin** provided on said insulating material **such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin**."

The Examiner alleged that Wojnarowski et al comprises a sealing resin (inherent) provided on said insulating material such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin.

Wojnarowski et al, however, discusses nothing about such sealing resin. Thus, Wojnarowski et al does not teach or suggest, among other things, "a sealing resin provided on said insulating material such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin."

The Examiner recites that elements 31, 38 and 40 of Wojnarowski et al are chip terminals. According to Wojnarowski et al, elements indicated by reference numeral 31 are input/output terminals. Reference 38 indicates a power bus and reference 40 indicates a ground bus.

The Examiner also alleged that an element 40 is a non-test chip terminal. In Wojnarowski et al, however, reference numeral 40 indicates a ground bus and reference numeral 41 indicates a ground test pad (Fig. 15; Column 13, lines 48-53).

Therefore, Wojnarowski et al does not disclose that the distribution trace connected to a test terminal is extended out of the semiconductor chip circuit forming region and that a testing member is formed outside the semiconductor chip circuit forming region. With the structure of Wojnarowski et al, a test is performed only using a power terminal, a ground terminal and a signal terminal.

According to the present invention, since the redistribution trace is extended outside the semiconductor chip circuit forming region, a test can be performed using the test chip terminals.

For at least these reasons, claim 1 patentably distinguishes over Wojnarowski et al. Claims 2 and 3, directly depending from claim 1, also patentably distinguish over the cited reference for at least the same reasons.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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